IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

For:

WARREN M. FARNWORTH SALMAN AKRAM

Serial No.: 09/844,532

Filing Date: April 30, 2001

METHOD FOR FABRICATING A TEST

INTERCONNECT FOR BUMPED SEMICONDUCTOR COMPONENTS BY FORMING RECESSES AND CANTILIVERED LEADS ON A SUBSTRATE

(AS AMENDED)

Attorney Docket No. 97-1433.1

EXAMINER: Chang, R.

Art Unit: 3729

ΓΕCHNOLΦGY CENTER R3700

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

January 20, 2004

Mail Stop RCE
Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The citations listed on the accompanying Form PTO/SB/08, copies attached, may be material to the examination of the subject application and are therefore submitted in compliance with the duty of disclosure defined in 37 CFR §§1.56, 1.97 and 1.98.

This Information Disclosure Statement under 37 CFR §§1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional material to the examination of this application does not exist, or that any one or more of these citations constitutes prior art under 35 USC §102.

It is requested that the above citations be made of record, if appropriate, in the prosecution of this application.

Respectfully submitted:

Stephen A. Gratton, Reg. No. 28,418 Attorney of Record

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CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to: Mail Stop RCE, Commissioner For Patents, PO BOX 1450, Alexandria, VA 22313-1450 on this 20th day of January, 2004.

Date of Signature

Stephen A. Gratton, Attorney for Applicants